

SUB-MICRON MOS TRANSISTOR

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Cross-Reference to Related Applications

This application is a divisional of application Serial No. 09/783,760, filed February 14, 2001, entitled "Structure and Method of Making a Sub-Micron MOS Transistor,"
invented by Ma *et al*, which is a continuation-in-part of application Serial No. 09/004,991, filed January 9, 1998, now issued as U.S. Letters Patent No. 6,274,421 entitled "Method of Making Metal Gate Sub-Micron MOS Transistor," invented by Hsu *et al*.

Field of the Invention

This invention relates to MOS Transistor and IC fabrication method, and specifically to the use of a nitride undercut to form a sub-micron MOS.

Background of the Invention

The use of chemical etching to provide a controllable undercut has been used to produce conventional MOS transistors, which is known as a "T-gate" structure. A nitride undercut, using phosphoric acid, has been used specifically in the fabrication of triple implanted bipolar transistors, however, this process is not widely used now because of controllability issues required to manufacture ICs using current technology. The nitride undercutting process may remain a useful process in a certain application, such as in the manufacture of sub-micron MOS transistors.

Lightly doped (LDD) structures are widely used in state-of-the-art IC fabrication. The usual LDD process requires two implantation steps, however, one of the implantation steps is eliminated using the LDD method of the invention.

Summary of the Invention

A method of fabricating a sub-micron MOS transistor includes preparing a substrate, including isolating an active region therein; depositing a gate oxide layer; depositing a first selective etchable layer over the gate oxide layer; depositing a second selective etchable layer over the first selective etchable layer; etching the structure to undercut the first selective etchable layer; implanting ions in the active region to form a source region and a drain region; depositing and planarizing the oxide; removing the remaining first selective etchable layer and the second selective etchable layer; depositing a gate electrode; and depositing oxide and metallizing the structure

A sub-micron MOS transistor includes a substrate; and an active region, including a gate region having a length of less than one micron; a source region including a LDD source region; and a drain region including a LDD drain region.

An object of the invention is to provide a method of fabrication for sub-micron transistors.

Another object of the invention is to provide a simplified LDD process.

This summary and objectives of the invention are provided to enable quick comprehension of the nature of the invention. A more thorough understanding of the invention may be obtained by reference to the following detailed description of the preferred embodiment of the invention in connection with the drawings.

Brief Description of the Drawings

Figs. 1-4 depicts steps in the method of the invention.

Fig. 5 depicts a sub-micron MOS transistor constructed according to the method

of the invention.

Detailed Description of the Preferred Embodiment

An n-channel MOS transistor is used as an example to describe the method of the invention, however, the structure and fabrication process is also applicable to p-channel MOS transistors and CMOS integration.

Referring to Fig. 1, a structure 10 constructed according to the method of the invention is fabricated using state-of-the-art processes on a p-type substrate 12 to form an n-well, a p-well, to adjust the voltage threshold in an active region 14, and to provide device isolation, as by oxide regions 16.

Turning to Fig. 2, a gate oxide layer 18 is formed, and a layer of silicon nitride (Si_3N_4), or polysilicon, 20, also referred to herein as a first selective etchable layer is deposited to a thickness of between about 200 nm to 500 nm. A thin layer of oxide 22, also referred to herein as a second selective etchable layer, is deposited over the nitride layer to a thickness of between about 20 nm to 100 nm.

This is followed by photo lithography and anisotropic plasma etching of oxide layer 22 and silicon nitride, or polysilicon, layer 20, or polysilicon, wherein the etching stops at the level of gate oxide 18. Gate oxide layer 18 may be partially etched, or may be completely removed during this etching process. The remaining silicon nitride, or polysilicon, layer forms a replacement cast for a gate electrode, which will be formed in a subsequent step. Any remaining photoresist is then removed, resulting in the structure shown generally at 10 in Fig. 2.

Referring now to Fig. 3, nitride layer 20 is partially etched using phosphoric acid, which has a high selectivity over oxide, *i.e.*, the phosphoric acid will remove silicon nitride

considerably faster than it will remove silicon oxide, resulting in the structure of Fig. 3. The gate length is shortened by two-times the thickness of the nitride etched, resulting in a device having a shorter channel, for instance, a gate length of 100 nm results from an initial nitride deposition having a length of 200 nm, of which 50 nm is removed by etching.

5 In the case where polysilicon is used as a replacement cast, the gate oxide must not be completely removed during the gate etching process. Polysilicon may be selectively etched by using diluted HNO_3 /HF solution. Additionally, the oxide layer 22 may be replaced with silicon nitride to achieve higher etching selectivity. In this case, silicon nitride is deposited to a thickness of between about 20 nm to 100 nm.

10 A source region 24 and a drain region 26 is formed in active region 16 by ion implantation adjacent a gate region 27. In the preferred embodiment, Arsenic ions are implanted at a dose of between about $1 \cdot 10^{15} \text{ cm}^{-2}$ to $5 \cdot 10^{15} \text{ cm}^{-2}$, and an energy level of between about 30 keV to 70 keV. Because of overhanging oxide 22, the implantation depth and dose is reduced in the region under the overhanging oxide, which results in an LDD source region 24a and an LDD
15 drain region 26a adjacent gate region 27, without an additional implantation step. The implanted profile in this region is a function of implant energy, dose, and the thickness of the oxide. For instance, the ion concentration in the source region 24 and drain region 26 is between about $1 \cdot 10^{20} \text{ cm}^{-3}$ to $1 \cdot 10^{21} \text{ cm}^{-3}$, while the ion concentration in LDD source region 24a and LDD drain region 26a is between about $5 \cdot 10^{18} \text{ cm}^{-3}$ to $5 \cdot 10^{19} \text{ cm}^{-3}$. The gate may be heavily doped
20 polysilicon or metal.

 The next step is to CVD an oxide layer 28 to a thickness of between about 1.5 times to two times the thickness of silicon nitride layer 20. The structure is planarized by CMP,

stopping at the level of silicon nitride layer 20. A high selectivity slurry is desirable for this process. Nitride layer 20 is etched to remove it, and doped polysilicon or metal 30 is deposited and CMP planarized to form a gate electrode. An oxide layer 32 is deposited by CVD, and a source electrode 34 and a drain electrode is formed, resulting in the structure shown generally at 38 in Fig. 5.

The remainder of the process proceeds as described in an earlier patent disclosure by Hsu and Evans describing the nitride replacement or "cast" process. For conventional polysilicon gate fabrication, standard processing, which is well known to those of ordinary skill in the art, is performed.

Thus, a structure and a method for fabricating a sub-micron MOS transistor using a silicon nitride or polysilicon undercut process has been disclosed. It will be appreciated that further variations and modifications thereof may be made within the scope of the invention as defined in the appended claims.